EFFECT OF DISTRIBUTED GATE DIODE ON MESFET POWER PERFORMANCE EVALUATED BY HARMONIC BALANCE SIMULATION

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ABSTRACT

A mechanism for power limitation in GaAs MESFETs which arises from the distributed conduction properties of the resistive gate diode is evaluated using harmonic balance simulation in conjunction with a distributed diode model. It is shown that 1 dB compressed power output and peak efficiency depend on unit gate finger width which has significance for device layout and choice of gate technology in high-power applications. The simulation results are supported by experimental data.

INTRODUCTION

A mechanism has been identified for power limitation in GaAs MESFETs which is a consequence of the distributed conduction properties of the gate diode at high drive levels. The magnitude of the effect depends on gate metallization resistance and unit gate finger width thus it has implications for the layout and choice of gate technology for high-power and high-efficiency applications. In this paper the mechanism is evaluated as a function of gate finger width for a typical half-micron gate X-band power FET by combining harmonic balance simulation with a distributed analysis of the conducting gate diode. Power output at 1 dB compression is predicted to be reduced by 50 mW/mm and power-added efficiency by 8 percentage points when gate finger width is increased from 50 microns to 200 microns. Experimental data is presented which qualitatively confirms these results.

POWER LIMITING MECHANISM

It is well known that gain compression and power saturation in properly matched GaAs MESFETs is accompanied by the appearance of gate conduction current as the gate diode is driven into forward conduction and sometimes also into reverse avalanche breakdown at the extremes of the RF cycle. Figure 1 shows power output and average DC gate current plotted against power input for a typical power FET. In this 18 GHz device example the forward conduction current overcomes the avalanche current and dominates as the RF drive increases. Although average DC current is typically in the range 1 to 10 mA/mm at 1 to 2 dB compression for a normally biased FET in class A or AB operation, the conduction current flow is actually limited to only a small fraction of the RF cycle and instantaneous currents can be as high as 100 to 200 mA/mm. This current flows through the resistive gate metallization giving rise to substantial voltage drops which cause regions of the gate remote from the input end to receive a reduced drive and consequently contribute less power to the total output. The situation is illustrated in the FET channel schematic of Figure 2 which shows how instantaneous voltage V at gate-width element ΔW is reduced below the input voltage V_0 because of the potential drop down the rest of the gate. This internal voltage drop mechanism occurs only when the gate is driven into conduction or avalanche breakdown. It is quite distinct from transmission line effects (1) which attenuate the input signal at all drive levels and cause small signal gain reduction.

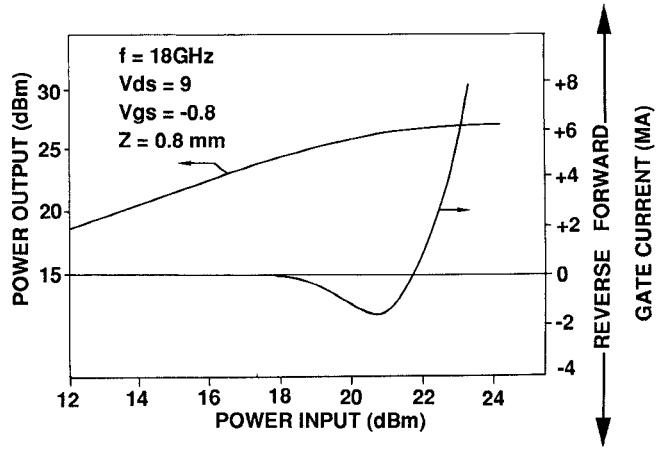

Figure 1. Typical Dependence of Average Gate Current on RF Power Input for a MESFET Driven into Gain Compression; Example for Ku-Band Power FET.

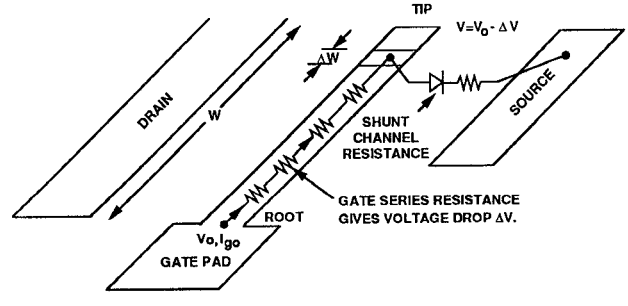

Figure 2. Schematic Representation of Conducting Gate Finger showing Origin of Internal Self-Biasing for Element ΔW.

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Analysis of the consequences of this mechanism for power performance was undertaken using a harmonic balance load-pull simulator "HARM"* and a program developed to evaluate the voltage distribution on a conducting gate diode finger. In the interests of simplicity only forward conduction of the diode was considered in this work, justified by the observation that forward conduction generally dominates under normal operation.

ANALYSIS OF DISTRIBUTED DIODE

The distributed nature of the gate diode finger was analysed using the ladder type network representation shown in Figure 3. Each section is characterized by an elemental Schottky diode, series resistance R_s, and shunt resistance parameter R_p. These resistances are scaled from the series gate finger resistance per unit width R_o ohm/mm and a shunt channel resistance R_c ohm mm which is roughly equivalent to source resistance plus gate charging resistance R_i. A computer program was written using the full Schottky diode equation to solve the network for all currents and voltages at any specified input voltage V_o. A few trials showed that a section width of 10 microns was sufficiently small to give an accurate representation of the distributed gate properties. Of particular interest in this investigation was the effect of gate finger width on voltage distribution. Figure 4 shows computed results for finger widths ranging from 50 to 300 microns at an applied input voltage of 1.2 volts. These were calculated using gate resistance of 250 ohm/mm and shunt resistance of 2 ohm mm which are representative of the FETs modelled for the large signal simulation. A forward bias of 1.2 volts is typical of the peak value achieved at the open channel end of the current swing under high RF drive. It is apparent that under these conditions there is a substantial voltage drop towards the tip of the wider fingers.

HARMONIC BALANCE SIMULATION

The simulator "HARM" evaluates power and efficiency under any specified bias and drive conditions after first establishing the optimum load and input match. It also provides the internal gate and drain waveforms. "HARM" accepts a number of standard large signal models including the "Curtice-Ettenberg" (2) model which was adopted in this work. The model was derived for a group of moderate performance half-micron gatelength X-band power FETs by standard s-parameter and I-V measurement techniques using in-house parameter extraction software. It is important to emphasize that the large signal model is a lumped representation. Scaling to different unit finger widths for devices of the same periphery is accomplished simply by appropriately changing effective gate resistance R_g as in a small signal model. This has an effect on small signal gain in the simulation but but does not change the power saturation behavior.

The method used to evaluate the effect of the distributed gate diode is explained using the example of a 1mm FET constructed from 100 micron gate fingers. The FET, shown schematically in Figure 5, is sliced into ten hypothetical sections. According to the conventional lumped representation, output power contributed by each of the sections at a particular input power is just one tenth of the total since it is implicitly assumed that the input drive to each section is the same. The average attenuation of the input signal is

* HARM is a commercially available simulator from W.R. Curtice Consulting.

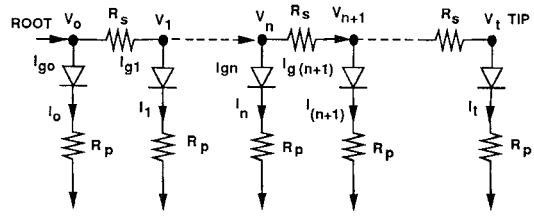

Figure 3. Ladder-Type Network Representation of Distributed Gate Diode in Forward Conduction.

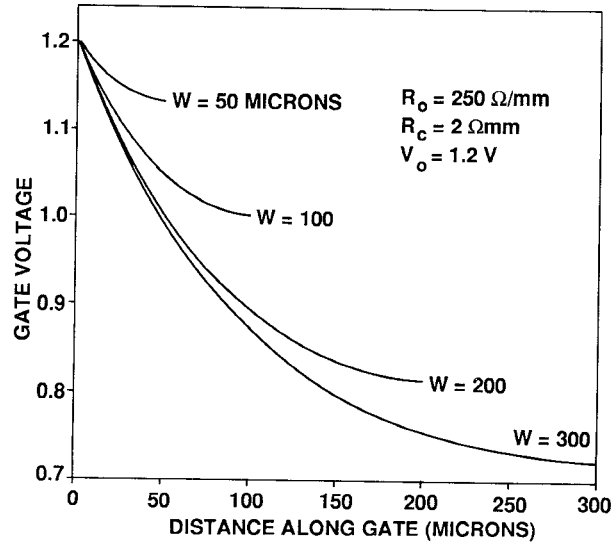

Figure 4. Voltage Distribution on Gate Diode Raised to +1.2V at Input End Evaluated as a Function of Finger Width.

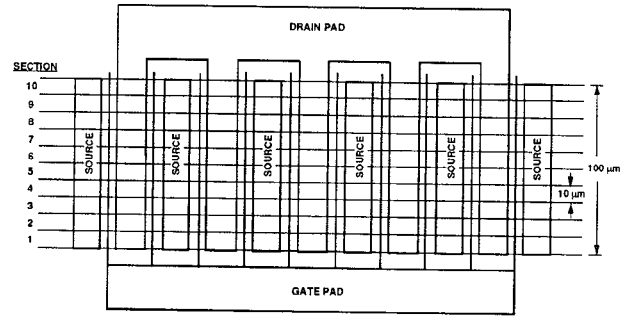

Figure 5. Schematic Representation of 1mm Periphery Power FET Composed of 100 Micron Fingers Showing Decomposition into Ten Hypothetical Slices for Simulation of Distributed Diode Effects.

accounted for by the effective gate resistance R_g in the model. A run of "HARM" simulations over the full range of power input from small signal to saturation gives the lumped model transfer characteristic. However, it is apparent that the input waveforms enable a plot of power output versus peak input voltage also to be constructed. This plot is shown in Figure 6 for the 100 micron gate finger device. The power is constrained to saturate at 0.9 volts peak input because this corresponds to peak drain current reaching the full open channel value I_{max} for these devices. (Power saturation is introduced into the plot because the current control equations generate currents which are in excess of I_{max}. This is a shortcoming of all existing large signal models.) At lower drive the power varies approximately linearly with gate voltage as would be expected for drain current changes in a region of approximately constant transconductance.

At any power input the peak gate voltage from the simulation can be used as the input in the distributed diode program to determine the peak voltage at each of the gate sections. The corresponding output powers are read from the plot of Figure 6 and are summed to give the total for the device. This is repeated at each power input to construct the distributed model power transfer characteristic. A similar procedure applied to the average drain current enables efficiency curves also to be plotted.

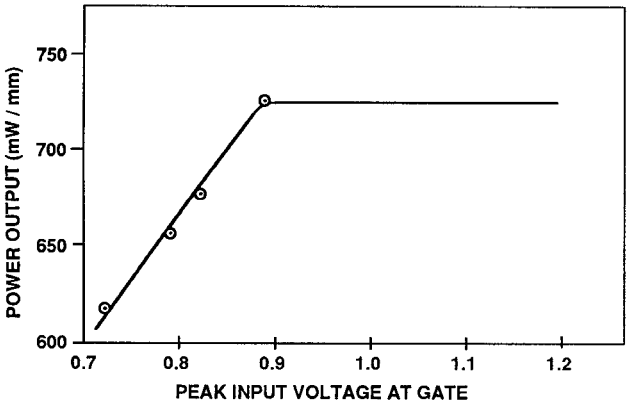

Figure 6. Power Output Plotted against Peak Input Voltage from "HARM" Simulation of 10 x 100 Micron FET at 12 GHz.

RESULTS

The procedure outlined above was applied to 1mm periphery FETs constructed with 50, 100, 167 and 200 micron gate fingers. Bias conditions were V_{ds}=7 and V_{gs}=-1.5 with simulation frequency of 12 GHz. The power transfer and efficiency characteristics according to both lumped and distributed simulations are shown in Figure 7 for the two extreme cases of 50 micron and 200 micron finger width. The effect of gate resistance on small signal gain is immediately apparent in comparing the plots but the phenomenon of interest here is the power saturation behavior. It is clear that for the case of 50 micron gate fingers there is little difference between the distributed and lumped simulations. At 200 microns however the distributed result shows a significantly earlier onset of compression, a reduced 1 dB compressed power and a lower efficiency. In Figure 8 power at 1 dB compression is plotted against gate finger width using results from all four simulations. The lumped model predicts nearly constant output power as expected whereas the distributed model shows a reduction from 680 mW/mm to 628 mW/mm as the gate is widened to 200 microns. Peak efficiency versus finger width is plotted in Figure 9. Both models show a decrease with finger width caused by the effect of gain but the total reduction is 2.5 percentage points greater for the distributed case.

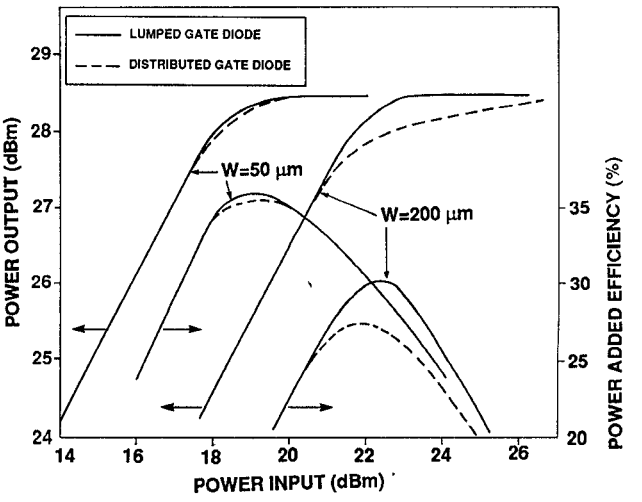

Figure 7. Simulated 12 GHz Performance of X-Band Power FETs Constructed with 50 Micron and 200 Micron Unit Gate Fingers. Results are Compared using the Distributed and Conventional Lumped Representations of the Gate Diode.

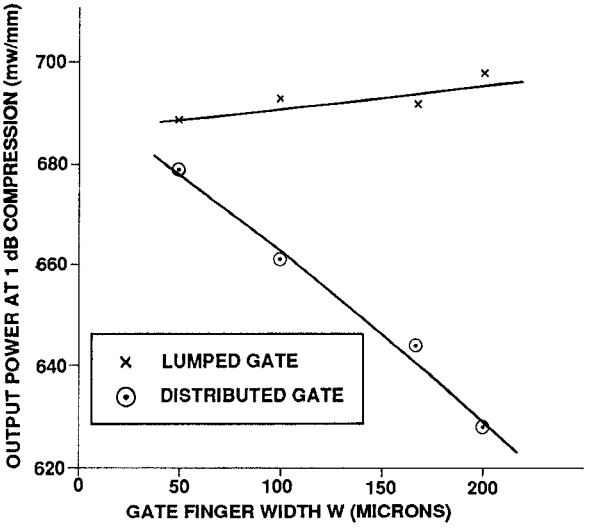

Figure 8. Simulated Power Output per mm at 12 GHz and 1 dB Compression for X-Band Power FETs as a Function of Unit Gate Finger Width Comparing Distributed and Conventional Lumped Representations of the Gate Diode.

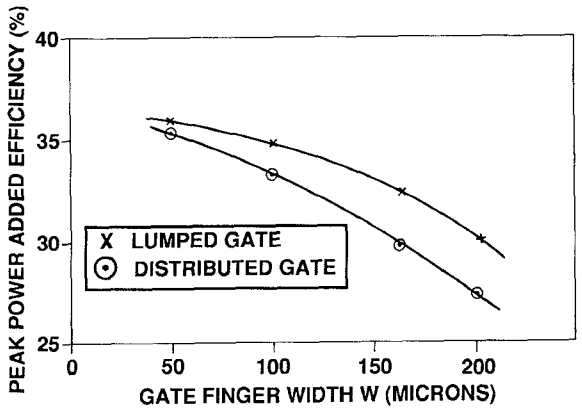

Figure 9. Simulated Peak Power-Added Efficiency at 12 GHz for X-Band Power FETs as a Function of Unit Gate Finger Width Comparing Distributed and Lumped Representations of the Gate Diode.

Experimental data to support the simulation results is presented in Table 1. The measurements pertain to a controlled experiment in which 2mm periphery X-band power FETs designed with 80, 140 and 200 micron gate fingers were included on a single maskset. The table gives averaged performance data for a number of devices from a single wafer tuned for maximum efficiency at 10 GHz and 6V drain bias. The power output shows a decrease of 43 mW/mm, and efficiency drops by 8.5% when finger width is increased from 80 to 200 microns. Allowing for the differences in frequency and bias these results are in good qualitative agreement with the simulations.

Table 1. Experimental Data Showing Dependence of Power and Efficiency on Gate Finger Width for X-Band FETs.

V_{ds} = 6, f = 10 GHz

Gate Finger Width (Microns)	Power at Peak Efficiency (mW/mm)	Peak Power-Added Efficiency (%)
80	537	43.8
140	525	40.7
200	494	35.4

CONCLUSIONS

It has been shown that power saturation in GaAs MESFETs is affected by the distributed nature of the gate diode. The mechanism is the appearance of voltage drops along the width of the resistive finger when the gate is driven into forward conduction or avalanche breakdown under high RF drive. The effect has been evaluated for forward conduction by combining harmonic balance simulation with a distributed analysis of the gate diode. Simulations for a typical X-band FET showed that 1 dB compressed power output and peak efficiency decreased with increasing gate finger width. The predicted power reduction of 50 mW/mm and efficiency reduction of 8 percentage points when gate finger width was increased from 50 to 200 microns are supported qualitatively by experimental data. These conclusions have importance in the choice of layout and gate technology for high power applications of GaAs FETs and related devices. Thus low gate resistance, achieved with short fingers or by tee section structures, is important to maximize power as well as small signal gain. Finally, it is concluded that accurate large signal simulations at high drive levels should take account of this effect.

ACKNOWLEDGEMENTS

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